

HARYANA COLLEGE OF TECHNOLOGY AND MANAGEMENT, KAITHAL.

Lesson plan

IV SEMESTER IT JAN-MAY 2009

Course Handout

Details regarding the course lesson plan

Course No.: CSE-202E

Course Title: Computer Architecture & Organization

Instructor-in-charge: Er. Saurabh Mittal

Sessional: 50 Marks

Exam: 100 Marks

Total: 150 Marks

Duration of Exam: 3 Hrs.

Text and Reference:

1. Text Books:

- Computer Organization and Design, 2nd Ed., by David A. Patterson and John L. Hennessy, Morgan 1997, Kauffmann.
- Computer Architecture and Organization, 3rd Edi, by John P. Hayes, 1998, TMH.

2 Reference Books:

- Operating Systems Internals and Design Principles by William Stallings, 4th edition, 2001, Prentice-Hall Upper Saddle River, New Jersey.
- Computer Organization, 5th Edi, by Carl Hamacher, Zvonko Vranesic, 2002, Safwat Zaky.
- Structured Computer Organisation by A.S. Tanenbaum, 4th edition, Prentice-Hall of India, 1999, Eastern Economic Edition.

Note: Eight questions will be set in all by the examiners taking at least two questions from each unit .Students will be required to attempt five questions in all at least one from each unit.

3. Lecture Schedule:

Lecture	Topics	Date
Lecture 1	Store program control concept	2/2/09
Lecture 2	Flynn's classification of computers (SISD, MISD, MIMD)	4/2/09
Lecture 3	Multilevel viewpoint of a machine: digital logic, micro architecture	6/2/09
Lecture 4	ISA, operating systems, high level language	9/2/09
Lecture 5	Structured organization; CPU, caches, main memory, secondary memory units & I/O	11/2/09
Lecture 6	Performance metrics; MIPS, MFLOPS	13/2/09
Lecture 7	Instruction set based classification of processors (RISC, CISC, and their comparison)	16/2/09
Lecture 8	Addressing modes: register, immediate, direct, indirect, indexed; Operations in the instruction set; Arithmetic and Logical, Data Transfer, Machine Control Flow	18/2/09

Lecture 9	Instruction set formats (fixed, variable, hybrid); Language of the machine: 8086 ; simulation using MASM	20/2/09
Lecture 10	CPU Architecture types (accumulator, register, stack, memory/ register)	25/2/09
Lecture 11	Detailed data path of a typical register based CPU, Fetch-Decode-Execute cycle (typically 3 to 5 stage)	27/2/09
Lecture 12	Microinstruction sequencing, implementation of control unit, Enhancing performance with pipelining	2/3/09
Lecture 13	Hardwired control design method, Micro programmed control unit	4/3/09
Lecture 14	The need for a memory hierarchy (Locality of reference principle	6/3/09
Lecture 15	Memory hierarchy in practice: Cache, main memory and secondary memory	9/3/09
Lecture 16	Memory parameters: access/ cycle time, cost per bit); Main memory (Semiconductor RAM & ROM organization, memory expansion, Static & dynamic memory types)	20/3/09
Lecture 17	Cache memory (Associative & direct mapped cache organizations	23/3/09
Lecture 18	Allocation & replacement polices, segments, pages & file organization, virtual memory	25/3/09
Lecture 19	Goals of parallelism (Exploitation of concurrency, throughput enhancement)	27/3/09
Lecture 20	Amdahl's law; Instruction level parallelism (pipelining, super scaling – basic features)	30/3/09
Lecture 21	Processor level parallelism (Multiprocessor systems overview)	1/4/09
Lecture 22	Instruction codes, computer register, computer instructions	6/4/09
Lecture 23	Timing and control, instruction cycle, type of instructions	8/4/09
Lecture 24	Memory reference, register reference. I/O reference	10/4/09
Lecture 25	Basics of Logic Design, accumulator logic, Control memory	13/4/09
Lecture 26	Address sequencing, micro-instruction formats, micro-program sequencer	15/4/09
Lecture 27	Stack Organization, Instruction Formats, Types of interrupts	17/4/09
Lecture 28	Memory Hierarchy. Programmed I/O, DMA & Interrupts	27/4/09